

FIG. 2

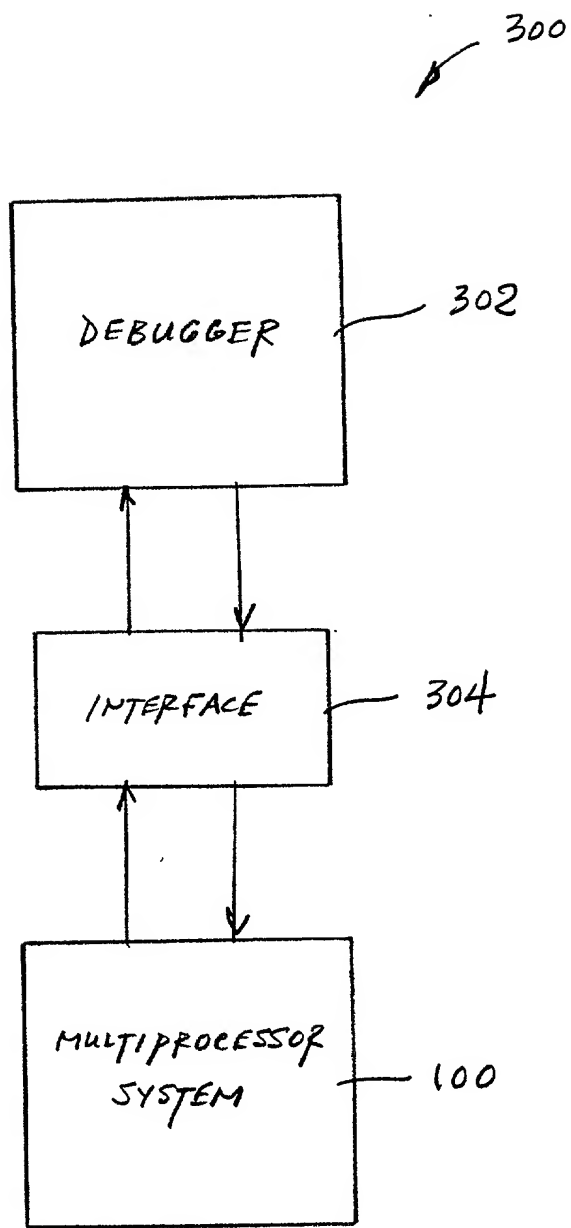


FIG. 3

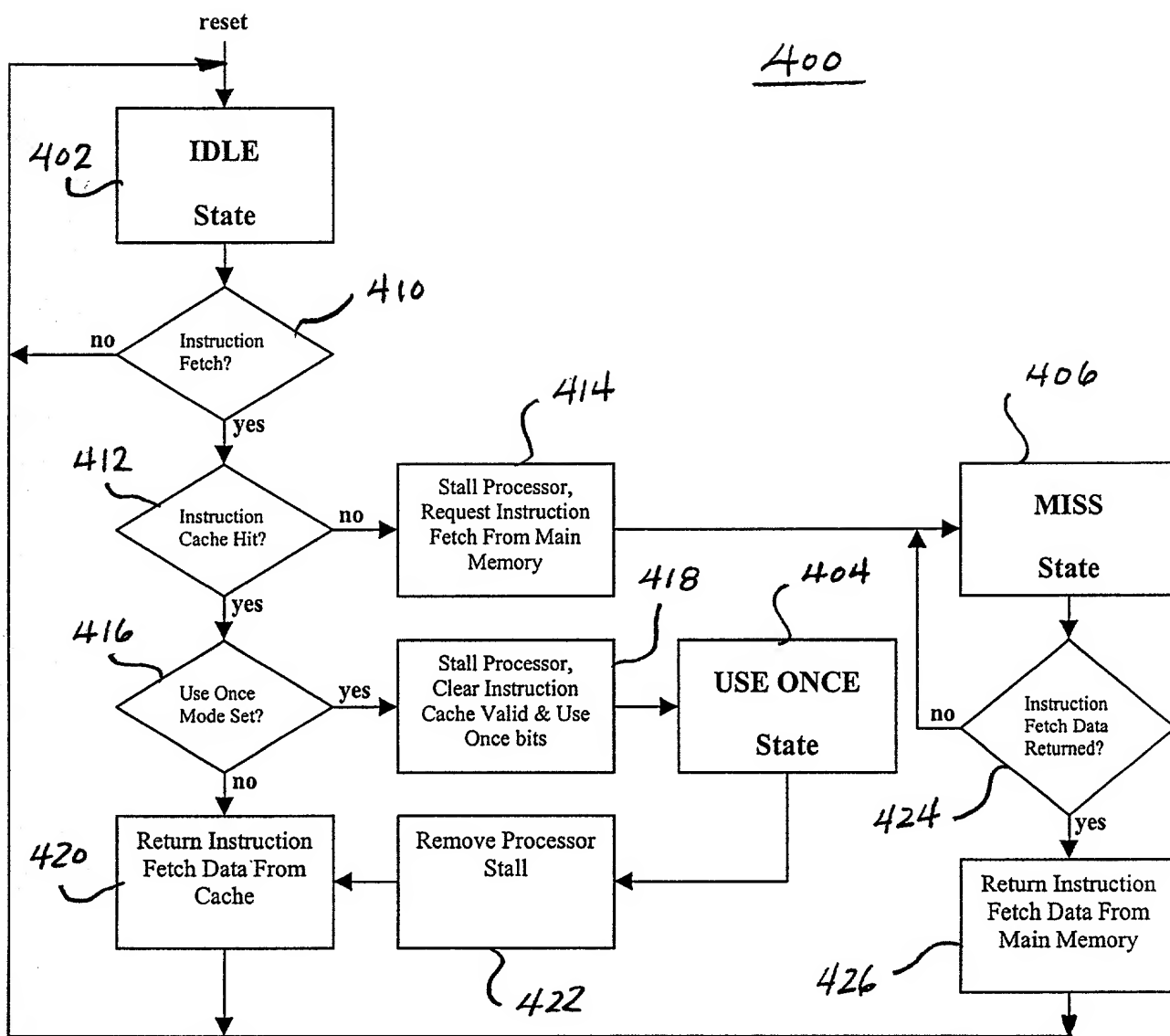


FIG. 4

P0 state: NONDEBUG
 P0 cache[index(swbpt)] V state: 0
 P0 cache[index(swbpt)] U state: 0
 P0 cache[index(swbpt)] Tag state: x
 P0 cache[index(swbpt)] Data state: x
 P1 state: NONDEBUG
 P1 cache[index(swbpt)] V state: 0
 P1 cache[index(swbpt)] U state: 0
 P1 cache[index(swbpt)] Tag state: x
 P1 cache[index(swbpt)] Data state: x
 P2 state: NONDEBUG
 P2 cache[index(swbpt)] V state: 0
 P2 cache[index(swbpt)] U state: 0
 P2 cache[index(swbpt)] Tag state: x
 P2 cache[index(swbpt)] Data state: x

(a)

P0 state: NONDEBUG
 P0 cache[index(swbpt)] V state: 1
 P0 cache[index(swbpt)] U state: 0
 P0 cache[index(swbpt)] Tag state: tag(swbpt)
 P0 cache[index(swbpt)] Data state: DEBUG
 P1 state: NONDEBUG
 P1 cache[index(swbpt)] V state: 0
 P1 cache[index(swbpt)] U state: 0
 P1 cache[index(swbpt)] Tag state: x
 P1 cache[index(swbpt)] Data state: x
 P2 state: NONDEBUG
 P2 cache[index(swbpt)] V state: 0
 P2 cache[index(swbpt)] U state: 0
 P2 cache[index(swbpt)] Tag state: x
 P2 cache[index(swbpt)] Data state: x

(b)

P0 state: DEBUG
 P0 cache[index(swbpt)] V state: 1
 P0 cache[index(swbpt)] U state: 0
 P0 cache[index(swbpt)] Tag state: tag(swbpt)
 P0 cache[index(swbpt)] Data state: DEBUG
 P1 state: NONDEBUG
 P1 cache[index(swbpt)] V state: 0
 P1 cache[index(swbpt)] U state: 0
 P1 cache[index(swbpt)] Tag state: x
 P1 cache[index(swbpt)] Data state: x
 P2 state: NONDEBUG
 P2 cache[index(swbpt)] V state: 0
 P2 cache[index(swbpt)] U state: 0
 P2 cache[index(swbpt)] Tag state: x
 P2 cache[index(swbpt)] Data state: x

(c)

P0 state: NONDEBUG
 P0 cache[index(swbpt)] V state: 1
 P0 cache[index(swbpt)] U state: 1
 P0 cache[index(swbpt)] Tag state: tag(swbpt)
 P0 cache[index(swbpt)] Data state: bpopcode
 P1 state: NONDEBUG
 P1 cache[index(swbpt)] V state: 0
 P1 cache[index(swbpt)] U state: 0
 P1 cache[index(swbpt)] Tag state: x
 P1 cache[index(swbpt)] Data state: x
 P2 state: NONDEBUG
 P2 cache[index(swbpt)] V state: 1
 P2 cache[index(swbpt)] U state: 0
 P2 cache[index(swbpt)] Tag state: tag(swbpt)
 P2 cache[index(swbpt)] Data state: DEBUG

(d)

FIG. 5

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P0 state: NONDEBUG
P0 cache[index(swbpt)] V state: 0
P0 cache[index(swbpt)] U state: 0
P0 cache[index(swbpt)] Tag state: x
P0 cache[index(swbpt)] Data state: x
P1 state: NONDEBUG
P1 cache[index(swbpt)] V state: 0
P1 cache[index(swbpt)] U state: 0
P1 cache[index(swbpt)] Tag state: x
P1 cache[index(swbpt)] Data state: x
P2 state: DEBUG
P2 cache[index(swbpt)] V state: 1
P2 cache[index(swbpt)] U state: 0
P2 cache[index(swbpt)] Tag state: tag(swbpt)
P2 cache[index(swbpt)] Data state: DEBUG
(e)

P0 state: NONDEBUG
P0 cache[index(swbpt)] V state: 0
P0 cache[index(swbpt)] U state: 0
P0 cache[index(swbpt)] Tag state: x
P0 cache[index(swbpt)] Data state: x
P1 state: NONDEBUG
P1 cache[index(swbpt)] V state: 0
P1 cache[index(swbpt)] U state: 0
P1 cache[index(swbpt)] Tag state: x
P1 cache[index(swbpt)] Data state: x
P2 state: NONDEBUG
P2 cache[index(swbpt)] V state: 1
P2 cache[index(swbpt)] U state: 1
P2 cache[index(swbpt)] Tag state: tag(swbpt)
P2 cache[index(swbpt)] Data state: bopcode
(f)

P0 state: NONDEBUG
P0 cache[index(swbpt)] V state: 0
P0 cache[index(swbpt)] U state: 0
P0 cache[index(swbpt)] Tag state: x
P0 cache[index(swbpt)] Data state: x
P1 state: NONDEBUG
P1 cache[index(swbpt)] V state: 0
P1 cache[index(swbpt)] U state: 0
P1 cache[index(swbpt)] Tag state: x
P1 cache[index(swbpt)] Data state: x
P2 state: NONDEBUG
P2 cache[index(swbpt)] V state: 0
P2 cache[index(swbpt)] U state: 0
P2 cache[index(swbpt)] Tag state: x
P2 cache[index(swbpt)] Data state: x
(g)

FIG. 5 (CONT'D)